REMARKS

This Amendment responds to the Office Action dated August 9, 2004 in which the Examiner rejected claims 1, 6, 7, 10 and 11 under 35 U.S.C. §102(b) and objected to claims 2-5 and 8-9 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, claim 1 has been amended to make explicit what is implicit in the claim. The amendment is unrelated to a statutory requirement for patentability. Additionally, claims 8, 9 and 11 have been rewritten into independent form. The Amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of claims 8, 9 and 11. Claim 10 has been amended merely for dependency due to the cancellation of claim 7. The Amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claim.

Claim 1 claims a modulator using a delta-sigma conversion method, and comprises component separating unit, delta-sigma modulator and output operating unit. The component separating unit separates a signal component and an error component of a digital input signal from each other. The delta-sigma modulator modulates the error component separated by the component separating unit. The output operating unit operates the signal component separated by the component separating unit and the error component modulated by the delta-sigma modulator.

Through the structure of the claimed invention separating a digital input signal into two components as claimed in claim 1, the claimed invention provides a modulator which can improve stability and precision. The prior does not show, teach or suggest the invention as claimed in claim 1.

Claim 11 claims a modulator using a delta-sigma conversion method, and comprises component separating unit, delta-sigma modular and output operating unit. The component separating unit separates a signal component and an error component of an input signal from each other. The delta-sigma modulator modulates the error component separated by the component separating unit. The output operating unit operates the signal component separated by the component separating unit and the error component modulated by the delta-sigma modulator. The component separating unit includes a multibit quantizer, digital-to-analog converter and an adder. The multibit quantizer quantizes an analog input signal to provide a multibit form. The digital-to-analog converts converting the signal component provided from the multibit quantizer to an analog signal. The adder adds the analog input signal to the analog signal provided from the digital-to-analog converter.

Through the structure of the claimed invention having a component separating unit including a multibit quantizer to provide a multibit form as claimed in claim 11, the claimed invention provides a modulator having improved stability. The prior art does not show, teach or suggest the invention as claimed in claim 11.

Claim 1 was rejected under 35 U.S.C. §102(b) as being anticipated by *Karema et al* (U.S. Patent No. 5,061,928).

Karema et al appears to disclose a method of cascading two or more sigma-delta modulators by applying an error signal representing the quantization error of a preceding modulator to a subsequent modulator in the cascade to be quantized therein, the quantized error signal being thereafter differentiated and subtracted from the quantized output signal of the preceding modulator. (col. 1, lines 8-14) The

system of FIG. 1 comprises two substantially identical second-order sigma-delta modulators A and B. (col. 3, lines 37-38) X is an analog input signal applied to the system. (col. 4, line 32)

Thus, *Karema et al* merely discloses modulators using an analog input signal. Nothing in *Karema et al* shows, teaches or suggests a modulator in which a digital input signal is provided as claimed in claim 1. Rather, *Karema et al* merely discloses an analog input signal applied to the system.

Since nothing in *Karema et al* shows, teaches or suggests a digital input signal as claimed in claim 1, applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claim 1 was rejected under 35 U.S.C. §102(b) as being anticipated by *Ritoniemi et al* (U.S. Patent No. 5,629,701).

Ritoniemi et al appears to disclose a method for cascading at least two sigma-delta modulators, wherein an error of one modulator in the cascade is quantized by the next modulator in the cascade; the quantized error is differentiated; and the differentiated error is subtracted from the quantized output signal of said one modulator. (col. 1, lines 6-11) In sigma-delta modulators (also known as delta-sigma modulators), the signal is quantized by using only a small number of quantization levels (2-256, which corresponds to an A/D converter with a resolution of 1 to 8 bits) at a high rate, usually 32-512 times the signal frequency. The ratio between the Nyquist sampling frequency (two times the useful signal band) and the used high sampling frequency is also called oversampling ratio (M). A quantizer is a combination of an A/D and a D/A converter, in which an analog signal is converted

by the A/D converter to a discrete digital value which is then immediately converted back to an analog voltage (value) by the D/A converter. (col. 1, lines 15-26)

Thus, *Ritoniemi et al* merely discloses an analog input signal. Nothing in *Ritoniemi et al* shows, teaches or suggests a digital input signal as claimed in claim 1. Rather, *Ritoniemi et al* is merely related to analog modulators having an analog input signal.

Since nothing in *Ritoniemi et al* shows, teaches or suggests a modulator in which a digital input signal is provided as claimed in claim 1, applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 1, 6, 7, 10 and 11 were rejected under 35 U.S.C. §102(b) as being anticipated by *Van Bavel et al* (U.S. Patent No. 4,862,169).

Applicants respectfully request the Examiner provide a corrected PTO-892 which lists *Van Bavel et al* as part of the Notice of References Cited.

Van Bavel et al appears to disclose oversampling data converters for performing A/D conversion. (col. 1, lines 20-21) Shown in FIG. 2 is an oversampled A/D converter 21. Generally, converter 21 comprises a first quantization loop 23 and a second quantization loop 24. Although two quantization loops are illustrated, it should be understood that the present invention may be extended to include additional quantization loops if desired. Quantization loop 23 has an input terminal for receiving an analog input signal labeled "X" coupled to a first input of a subtractor circuit 26. An output of subtractor circuit 26 is connected to a first input of an adder circuit 28. An output of adder circuit 28 is connected to an input of a delay circuit 30. An output of delay circuit 30 is connected to a second input of adder circuit 28. Adder circuit 28 and delay circuit 30 comprise an integrator 31. The output of adder circuit

28 is also connected to an input of a quantizer circuit 32 having a quantization error labeled "e1" associated therewith. An output of quantizer circuit 32 provides a signal labeled "Y1" and is connected to an input of a delay circuit 34. An output of delay circuit 34 is connected to an input of a D/A converter 36. An output of D/A converter 36 is connected to a second input of adder circuit 26. An output of adder circuit 28 is also connected to an input of a delay circuit 38. An output of delay circuit 38 is connected to a first input of a subtractor circuit 40. An output of D/A converter 36 is also connected to a second input of subtractor circuit 40. An output of subtractor circuit 40 provides a signal labeled "Z" and is connected to an input of an analog low pass filter circuit 42 having a transfer function labeled "H2". An output of filter circuit 42 is connected to an input of an amplifier circuit 44 having a gain labeled "G". Quantization loop 24 comprises a subtractor circuit 46 having a first input connected to an output of gain circuit 44. An output of subtractor circuit 46 is connected to a first input of an adder circuit 48. An output of adder circuit 48 is connected to a delay circuit 50. An output of delay circuit 50 is connected to a second input of adder circuit 48. Adder circuit 48 and delay circuit 50 comprise an integrator 51. An output of adder circuit 48 is connected to an input of a quantizer circuit 52 having a quantization error labeled "e2" associated therewith. An output of quantizer circuit provides a signal labeled "Y2" and is connected to an input of a delay circuit 54. An output of delay circuit 54 is connected to an input of a D/A converter 56. An output of D/A converter 56 is connected to a second input of adder circuit 46. An output of quantizer circuit 32 is connected to an input of a digital low pass filter circuit 60 having a transfer function labeled "H1". An output of filter circuit 60 is connected to an input of a delay circuit 62. An output of delay circuit 62 provides a signal labeled

"L" and is connected to a first input of an adder circuit 64. Adder circuit 64 provides a digital output signal labeled "Y" at an output thereof. An output of quantizer circuit 52 is connected to an input of a gain circuit 68 having a gain labeled "K". An output of gain circuit 68 is connected to an input of a differentiator circuit 70. An output of differentiator circuit 70 is connected to a second input of adder circuit 64. In operation, converter 21 receives an analog input signal X which may be represented graphically in FIG. 3A as a sinusoidal input signal. (col. 3, line 19 through col. 4, line 14)

Thus, *Van Bavel et al* merely discloses an analog input signal. Nothing in *Van Bavel et al* shows, teaches or suggests a digital input signal as claimed in claim 1.

Additionally, *Van Bavel et al* merely discloses a quantizer circuit 32. Nothing in *Van Bavel et al* shows, teaches or suggests a multibit quantizer which provides a multibit form as claimed in claim 11. Rather, *Van Bavel et al* merely discloses a quantizer.

Since nothing in *Van Bavel et al* shows, teaches or suggests a digital signal as claimed in claim 1 or a multibit quantizer as claimed in claim 11, applicants respectfully request the Examiner withdraws the rejection to claims 1 and 11 under 35 U.S.C. §102(b).

Claims 6 and 10 depend from claims 1 and 8 and recite additional features. Applicants respectfully submit that claims 6 and 10 would not have been anticipated by *Van Bavel et al* at least for the reasons as set forth above and since claim 10 now depends from an allowable claim. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 6 and 10 under 35 U.S.C. §102(b).

Since objected to claims 2-5 depend from allowable claims, applicants respectfully request the Examiner withdraws the objection thereto. Additionally, since objected to claims 8 and 9 have been rewritten into independent form, applicants respectfully request the Examiner withdraws the objection thereto.

New claim 12 has been added. Applicants respectfully submit that claim 10 is also in condition for allowance.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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